REMARKS

In response to the Office Action dated June 5, 2012, the Assignee respectfully requests reconsideration based on the above amendments and on the following remarks.

Claims 1 and 5-14 are pending in this application. Claims 15-51 have been, or previously were, canceled without prejudice or disclaimer.

Rejection under 35 U.S.C. § 112

The Office rejected claims 1, 5-14, 36, 39-46, and 52 under 35 U.S.C. § 112, first paragraph, for failing to comply with the written description requirement.

First, claims 36, 39-46, and 52 have been canceled without prejudice or disclaimer, so the rejection of these claims is moot.

Next, the rejection of the remaining claims 1 and 5-14 has been rendered moot by amendment. These claims have been amended to delete features for multiple buses, as Examiner Saltarelli notes in the rejection. Independent claim 1, instead, now recites features for a "*shared system bus*," which finds support in FIG. 2 and at page 16, lines 13-16. Processor, memory, and multiple pairs of a tuner and a demodulator connect to the shared system bus, and a data switch has multiple input ports and multiple output ports. These features are all supported by at least FIG. 2 and by page 16, lines 14-18 and by page 17, lines 20-end. Independent claim 1 also recites "*a dedicated link between one of the multiple input ports and one of the multiple pairs of the tuner and the demodulator, such that each pair of the multiple pairs of the tuner and the demodulator is dedicated to a different input port of the data switch.*" These features are all supported by at least FIG. 2 and by page 16, lines 7-13.

The Assignee, then, strongly asserts that the written description requirement is satisfied. The features recited by independent claim 1 are all fully supported by the embodiment of FIG. 2

and the cited passages. The Assignee, then, respectfully submits that the pending claims fully comply with the written description requirement of § 112, first paragraph. Removal of the rejection is respectfully requested.

Rejection of Claims under § 103 (a)

The Office rejected claims 1, 5-14, 36, 39-46, and 52 under 35 U.S.C. § 103 (a) as being obvious over U.S. Patent 6,005,861 to Humpleman in view of U.S. Patent 6,493,875 to Eames, *et al.*, in view of U.S. Patent 6,732,366 to Russo, further in view of U.S. Patent 4,890,168 to Inoue, *et al.*, and further in view of newly-cited U.S. Patent 6,967,962 to Medina, *et al.*

First, claims 36, 39-46, and 52 have been canceled without prejudice or disclaimer, so the rejection of these claims is moot.

Next, the rejection of remaining claims 1 and 5-14 is mistaken. The Examiner has, very respectfully, misinterpreted the newly-cited document to *Medina*. When *Medina* is correctly interpreted, the proposed combination of *Humpleman*, *Eames*, *Russo*, *Inoue*, and *Medina* still fails to teach or suggest all the features of the pending claims. One of ordinary skill in the art, then, would not think that claims 1 and 5-14 are obvious.

Medina has been misinterpreted. The Examiner concedes that *Humpleman*, *Eames*, *Russo*, and *Inoue* fails to teach or suggest a data switch with a dedicated port for each tuner/demodulator. So the Examiner proposes to add *Medina*. The Examiner specifically contends that *Medina* "dedicate[s] ports of an input switch to respective input devices." *See* Office Action mailed June 5, 2012 at page 9, lines 7-8.

This contention, though, is NOT what *Medina* teaches. *Medina* expressly explains that a port is dedicated to a switch:

As shown in FIG. 2, **cross bar 10 comprises a multiplicity of ports 16** which each port 16 comprises a link logic unit 18, an input FIFO buffer 20, a plurality of output buffers 22 and a port transmit arbiter 26. Typically cross bar 10 has four ports 16; however, it may comprise any number of ports 16.

Each port 16, and the elements which it comprises, are dedicated to an associated switch 12 or cross bar 10, and are responsible for all communication with its associated switch 12 or crossbar 10. As an example, the elements which comprise port 16A are associated with switch 12A and are responsible for switch 12A's communication: link logic unit 16A receives and directs messages and data from switch 12A, and performs various port functions which will be described in more detail hereinbelow; input FIFO buffer 20A receives and stores data packets sent from switch 12A; output buffers 22 at port 16A receive and store data packets sent to switch 12A; and, port transmit arbiter 26A sends messages and data to switch 12A.

See U.S. Patent 6,967,962 to Medina, *et al.* at column 3, lines 40-57 (emphasis added). Here *Medina* explains how a cross bar has multiple ports, and each port is dedicated to a different "switch." **That is, *Medina* dedicates a port to an entire switch**. *Medina* fails to realize that switches also have multiple ports, and that each individual port in the switch may be dedicated to a tuner and demodulator pair. *Medina* is thus wholly silent to "*a dedicated link between an input port of the switch and multiple pairs of the tuner and the demodulator, such that each pair of the multiple pairs of the tuner and the demodulator is dedicated to a different input port of the data switch*" (emphasis added). The proposed combination of *Humpleman*, *Eames*, *Russo*, *Inoue*, and *Medina* thus still fails to teach or suggest all the features of independent claim 1. One of ordinary skill in the art, then, would not think that independent claim 1 is obvious.

Moreover, independent claim 1 recites even more distinguishing features. As the above paragraph explained, *Humpleman*, *Eames*, *Russo*, *Inoue*, and *Medina* would dedicate a port in a cross bar to an entire switch. There is absolutely no teaching or suggestion of a dedicated input port to a "*tuner and demodulator*" pair. That is, *Humpleman*, *Eames*, *Russo*, *Inoue*, and *Medina* fails to teach or suggest "*a dedicated link between an input port of the switch and multiple pairs of the tuner and the demodulator.*" Because *Humpleman*, *Eames*, *Russo*, *Inoue*, and *Medina* is silent to all these features of independent claim 1, one of ordinary skill in the art would not think that independent claim 1 is obvious.

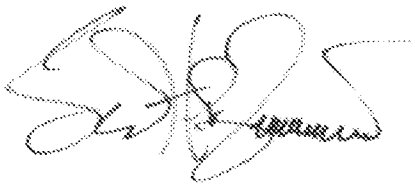
Yet independent claim 1 recites still more distinguishing features. Independent claim 1, for example, also recites "*a data switch having multiple input ports and multiple output ports*," and a "*dedicated link*" is established "*between an input port of the switch and multiple pairs of the tuner and the demodulator*" (emphasis added). The proposed combination of *Humpleman*, *Eames*, *Russo*, *Inoue*, and *Medina* wholly fails to teach a dedicated "*input*" port. The cited documents, instead, describe an "individual bus" between a cross bar port and the switch. *Medina* expressly explains how this bus sends and receives signals to "transfer" data between different switches. *See Medina*, at column 3, lines 16-17. Because *Humpleman*, *Eames*, *Russo*, *Inoue*, and *Medina* is silent to a dedicated "*input*" port, one of ordinary skill in the art would not think that independent claim 1 is obvious.

Claims 1 and 5-14, then, cannot be obvious over *Humpleman*, *Eames*, *Russo*, *Inoue*, and *Medina*. Independent claim 1 recites many distinguishing features, and the dependent claims incorporate these distinguishing features and recite even more features. One of ordinary skill in the art, then, would not think that these claims are obvious. The Office is respectfully requested to remove the § 103 (a) rejection of these claims.

If any questions arise, the Examiner is invited contact the undersigned at (919) 469-2629 or *scott@scottzimmerman.com*.

37 C.F.R. § 1.8 CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being electronically transmitted via the USPTO EFS web interface on August 30, 2012.



Scott P. Zimmerman
Attorney for the Assignee
Reg. No. 41,390